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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,486	02/07/2002	Jeffrey Alan Kash	YOR920010267US1 (14440)	1181

7590 10/02/2003

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EXAMINER	
PATEL, PARESH H	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,486	KASH ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kash et al. (US 5940545).

Regarding Claims 1, 8 and 13, Kash et al. (US 5940545) discloses: A system [fig. 1, 4] for testing an integrated circuit [5], comprising:

means [2] for obtaining periodic optical emissions over a defined period of time [fig. 2] and from a defined area [of an integrated circuit operating with time-varying internal currents;

means [3 and fig . 4]] for time-resolving said emissions by photon timing to estimate the number of switching events occurring in said defined area over said defined period;

means [lines 35-42 of column 6] for providing an optical emission model [fig. 1]; and

means [7 or 8] for comparing the optical emission from the area of the integrated circuit with the optical emission model to determine whether any of a group of defined conditions are present in the integrated circuit [lines 5-15 of column 7].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khurana (US 4680635) in view of Brahme et al.

Regarding Claims 1, 8 and 13, Khurana discloses: A system [an emission microscope] for testing an integrated circuit [silicon device], comprising:

means [11] for obtaining periodic optical emissions [the electroluminesent output of silicon 10] over a defined period of time [lines 56-65 of column 2 and 49-51 of column 6] and from a defined area of an integrated circuit [area of 10 where light emission from transistor, see lines 39-47 of column 6] operating with time-varying internal currents [input to 10 and lines 13-25 of column 6];

means [12, 13] for time-resolving said emissions by photon timing [lines 41-51 of column 6] to estimate the number of switching events occurring in said defined area over said defined period [inherent to determination of timing of the emission from the transistor and fast gating, see lines 28-51 of column 6];

means [14] for providing an optical emission model [lines 42-44 of column 4]; and

means [14] for comparing the optical emission from the area of the integrated circuit with the optical emission model to determine whether any of a group of defined

conditions are present in the integrated circuit [lines 42-44, 51-54 of column 4 and 48-51 of column 8].

Khurana also discloses (for claim 13) A program storage device [18, 19] readable by machine [14], tangibly embodying a program of instructions executable by the machine [lines55-68 of column 7] to perform above method steps.

Khurana discloses all the elements including an integrated circuit operating with internal current [input to 10 and lines 13-25 of column 6]. Khurana does not disclose an integrated circuit operating with **time-varying internal currents.** Brahme et al. discloses an integrated circuit operating with **time-varying internal currents** [application of test vectors, see lines 59-63 of column 6 or variation in clock speed to DUT from tester as further disclosed at lines 26-29 of column 4 and lines 31-36, 59-63 of column 6]. It would have been obvious to modify Khurana with time-varying input to internal circuit as taught by Brahme, in order to quickly pinpoint faults in a device (integrated circuit).

Regarding claims 2, 9 and 14, Khurana discloses: wherein the group of defined conditions include local power supply loading under high power density operation, and changes in switching performance due to heating effects [see different phenomena in abstract], and mid-cycle false switching, and effectiveness of switching control circuitry, and leakage control circuitry [lines 39-51 of column 6].

Regarding claims 3, 10 and 15, Khurana discloses: wherein: the obtaining means includes means for applying a given set of instruction vectors to the integrated circuit to

provide calibrated optical emissions [lines 37-55, particularly 53-55 of column 3 and instruction vector is inherent to 13-15 because device is calibrated]; and

the time-resolving means includes means for comparing said obtained optical emissions with said calibrated optical emissions [inherent to time resolution and intensifier means, see lines 9-13 of column 6 and 60-63 of column 5].

Regarding claims 4, 11 and 16, Khurana discloses: wherein the integrated circuit is used with a power distributing system [system that supplies current to 10] having a given time constant [inherent to current supply system] , and wherein the time resolving means [12,13] includes means for time resolving said emissions at a resolution greater than said time constant [inherent to 12, 13 in order to provide grater resolution, see lines 17-40, particularly 31-40 of column 5].

Regarding claims 5, 12 and 17, Khurana discloses: wherein the integrated circuit has a thermal time constant [inherent to integrated circuit also see lines 57-60 of column 6], and the time resolving means includes means for time resolving said emissions at a resolution greater than said thermal time constant [lines 52-68 of column 6].

Regarding claim 6, Khurana discloses: A method according to Claim 1, wherein the defined area includes groups of switches [transistors, lines 39-51 of column 6], each of said groups having a unique signature emission waveform [different wavelength of light emission], and the comparing step includes the step of searching the optical emissions from the area for any of the signature emission waveforms of said groups [lines 39-47 of column 6].

Regarding claim 7, Khurana discloses: A method according to Claim 6, wherein each of said groups of switches is comprised of a set of spatially unresolved individual gates [gates of the transistors].

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khurana (US 4680635) in view of Prasad [EP 0 639 778 A2]

Regarding Claims 1, 8 and 13, Khurana discloses: A system [an emission microscope] for testing an integrated circuit [silicon device], comprising:

means [11] for obtaining periodic optical emissions [the electroluminesent output of silicon 10] over a defined period of time [lines 56-65 of column 2 and 49-51 of column 6] and from a defined area of an integrated circuit [area of 10 where light emission from transistor, see lines 39-47 of column 6] operating with time-varying internal currents [input to 10 and lines 13-25 of column 6];

means [12, 13] for time-resolving said emissions by photon timing [lines 41-51 of column 6] to estimate the number of switching events occurring in said defined area over said defined period [inherent to determination of timing of the emission from the transistor and fast gating, see lines 28-51 of column 6];

means [14] for providing an optical emission model [lines 42-44 of column 4]; and

means [14] for comparing the optical emission from the area of the integrated circuit with the optical emission model to determine whether any of a group of defined conditions are present in the integrated circuit [lines 42-44, 51-54 of column 4 and 48-51 of column 8].

Khurana also discloses (for claim 13) A program storage device [18, 19] readable by machine [14], tangibly embodying a program of instructions executable by the machine [lines55-68 of column 7] to perform above method steps.

Khurana discloses all the elements including an integrated circuit operating with internal current [input to 10 and lines 13-25 of column 6]. Khurana does not disclose an integrated circuit operating with **time-varying internal currents.** Prasad discloses integrated circuit [10] operating with **time-varying internal currents** [pulse from 18, also see abstract]. Prasad also discloses microscope [14] for optical emission, detector 16 and determines switching [lines 11-14 of column 2 and 19-24 of column 3]. It would have been obvious to system of Khurana with time-varying internal current as taught by Prasad in order to detect which active elements of the integrated circuit are "on" or "off", which elements "latch up", and which elements "oscillate" contrary to expectations [see abstract].

Regarding claims 2, 9 and 14, Khurana discloses: wherein the group of defined conditions include local power supply loading under high power density operation, and changes in switching performance due to heating effects [see different phenomena in abstract], and mid-cycle false switching, and effectiveness of switching control circuitry, and leakage control circuitry [lines 39-51 of column 6].

Regarding claims 3, 10 and 15, Khurana discloses: wherein: the obtaining means includes means for applying a given set of instruction vectors to the integrated circuit to provide calibrated optical emissions [lines 37-55, particularly 53-55 of column 3 and instruction vector is inherent to 13-15 because device is calibrated]; and

the time-resolving means includes means for comparing said obtained optical emissions with said calibrated optical emissions [inherent to time resolution and intensifier means, see lines 9-13 of column 6 and 60-63 of column 5].

Regarding claims 4, 11 and 16, Khurana discloses: wherein the integrated circuit is used with a power distributing system [system that supplies current to 10] having a given time constant [inherent to current supply system] , and wherein the time resolving means [12,13] includes means for time resolving said emissions at a resolution greater than said time constant [inherent to 12, 13 in order to provide grater resolution, see lines 17-40, particularly 31-40 of column 5].

Regarding claims 5, 12 and 17, Khurana discloses: wherein the integrated circuit has a thermal time constant [inherent to integrated circuit also see lines 57-60 of column 6], and the time resolving means includes means for time resolving said emissions at a resolution greater than said thermal time constant [lines 52-68 of column 6].

Regarding claim 6, Khurana discloses: A method according to Claim 1, wherein the defined area includes groups of switches [transistors, lines 39-51 of column 6], each of said groups having a unique signature emission waveform [different wavelength of light emission], and the comparing step includes the step of searching the optical emissions from the area for any of the signature emission waveforms of said groups [lines 39-47 of column 6].

Regarding claim 7, Khurana discloses: A method according to Claim 6, wherein each of said groups of switches is comprised of a set of spatially unresolved individual gates [gates of the transistors].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
Sep. 11, 2003

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